WBS 1.1 Silicon Subsystem

Abe Seiden
UC Santa Cruz

Organization

Institutions

SUNY Albany
Iowa State University
UC Berkeley/LBNL
University of New Mexico
Ohio State University
University of Oklahoma/Langston Univ.
UC Santa Cruz
University of Wisconsin

Management

1.1.1 Pixels (Gilchriese)
1.1.1.1 Mechanics/Services (Gilchriese, Anderssen)
1.1.1.2 Sensors (Seidel, Hoeferkamp)
1.1.1.3 Electronics (Einsweiler, Denes)
1.1.1.4 Hybrids (Skubic, Boyd, Gan)
1.1.1.5 Modules (Garcia-Sciveres, Goozen)

1.1.2 Silicon Strips (Seiden)
1.1.2.1 IC Electronics (Grillo, Spencer)
1.1.2.2 Hybrids (Ciocio, Senior Techs)
1.1.2.3 Modules (Haber, Senior Techs)

1.1.3 RODs (Jared, Joseph)

(Physicist, Engineer or Senior Tech)

ETC02 Cost Profile
Silicon - WBS Level 3

Silicon ETC 02 Access Profile (Project K$s)

WBS	FY01	FY02	FY03	FY04	FY05	FY06	Total
111 Pixel System		2,365.0	2,559.9	520.3	6.5		5,451.6
112 Silicon Strip		1,446.9	784.6				2,231.6
113 Read-out Drivers		1,143.0	275.9	51.2	1.1		1,471.2
1.1 Total (FY02$s)	0.0	4,954.9	3,620.4	571.5	7.6	0.0	9,154.4
1.1 Total (AY$s)	0.0	4,954.9	3,721.8	604.0	8.3	0.0	9,288.9

ETC02 Cost Comparison
Silicon - WBS Level 3

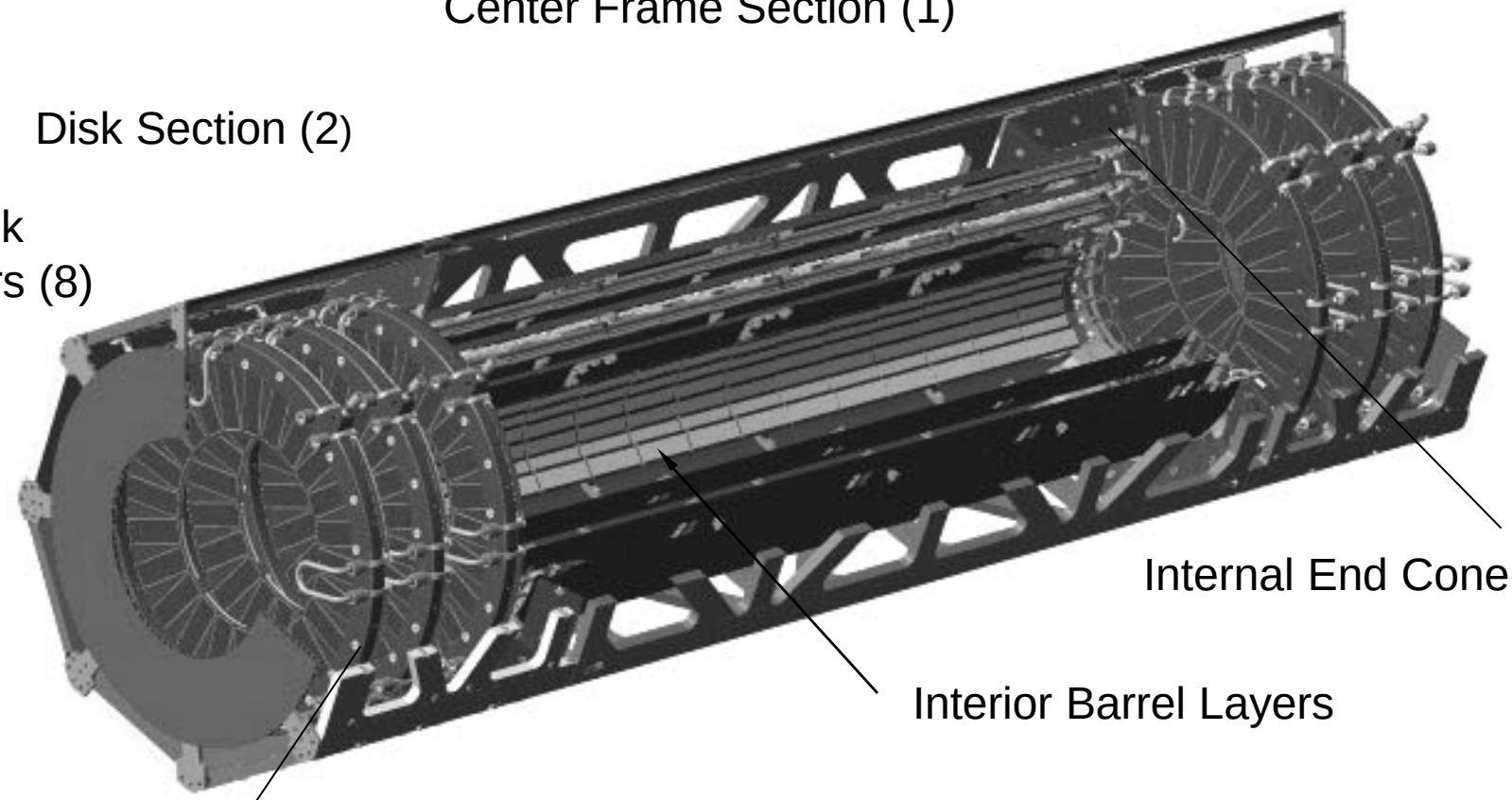
(Project AYk$s)

WBS	Baseline Budget (ETC01 FY02-FY05 + Carryover) Budget (AYk$s)	Final ETC02 (FY02-FY05) ETC Budget (AY$s)	Delta
111 Pixel System	5,243.4	5,553.4	(310.0)
112 Silicon Strip	1,844.4	2,253.5	(409.1)
113 Read-out Drivers	1,414.8	1,482.0	(67.2)
Total	8,502.6	9,288.9	(786.3)

1.1.1 Pixels - Overview

- The pixel system was baselined at the end of 2000. FY01 was the first year of baseline funding.
- Technical progress has been excellent in the last year
  - Working prototypes of all rad-hard, integrated circuits made and now under test
  - Silicon sensor production started
  - Mechanics production started
  - Module prototypes substantially advanced
- Schedule
  - Delay relative to baseline schedule of about 3 months in rad-hard ICs (critical path item). Sensor production and mechanics, expected completion as in baseline.
- Costs
  - TPC has increased. More engineering needed for ICs and related test systems. Diminished base program support projected.

Pixel System



(Services not shown)

Pixel System

2-Hit System - US Deliverables (Assumes release of management contingency).

- Mechanics(1.1.1.1)
  - Support tube and plugs at end of support tube
  - Overall pixel support structure(frame)
  - Disks
  - Coolant pipes(shared with Europe)
  - Power and other cables(shared with Europe)
  - Tooling for final assembly of system(shared with Europe)
- Sensors(1.1.1.2)
  - About 20% production procurement and testing
- Electronics(1.1.1.3)
  - About 20% production procurement, 50% of testing of front-end ICs
  - About 50% production procurement and testing of optical ICs
  - Common test systems for all collaboration for front-end ICs, modules
- Hybrids(1.1.1.4)
  - All flex hybrids
  - Optical components and hybrids for disk region
- Modules(1.1.1.5)
  - Thinning, dicing of FE and die sort
  - Assemble and test about 25% of modules
- Test Support(1.1.1.6)
  - About 20% of support for system tests and beam tests at CERN

Pixel System

Management Contingency

WBS	Desciption	Decision Date
1.1.1.2.3.1.2	Pixels Sensor	Done
1.1.1.2.3.1.3	Pixel Sensor testing (FY02 on)	Done
1.1.1.4.3.1.1	Bare Flex Hybrid Production	Late 02
1.1.1.4.3.1.2	Flex Components & Assembly	Late 02
1.1.1.3.3.1.1.2	FE IBM Production	Middle 03
1.1.1.4.3.3.2	Optical Hybrids	Middle 03
1.1.1.4.3.3.1	Optical Package & Component	Middle 03
1.1.1.5.3.3	FE IC die sort	Late 03
1.1.1.3.3.1.2	B-Layer Production	Early 04

Also from WBS 1.1.3 (RODs).

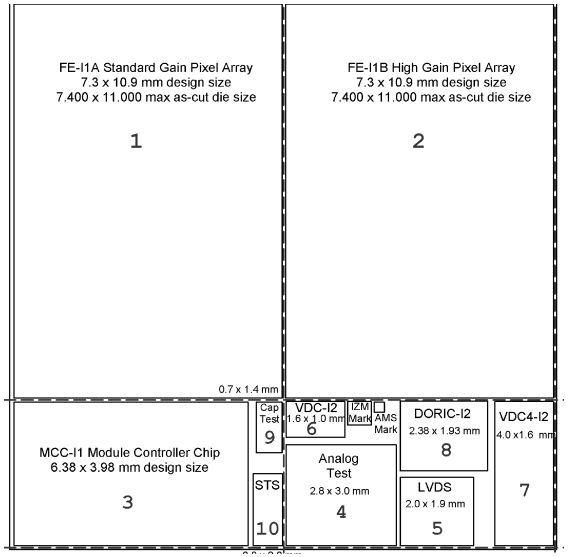
1.1.3.8	Pixel RODs

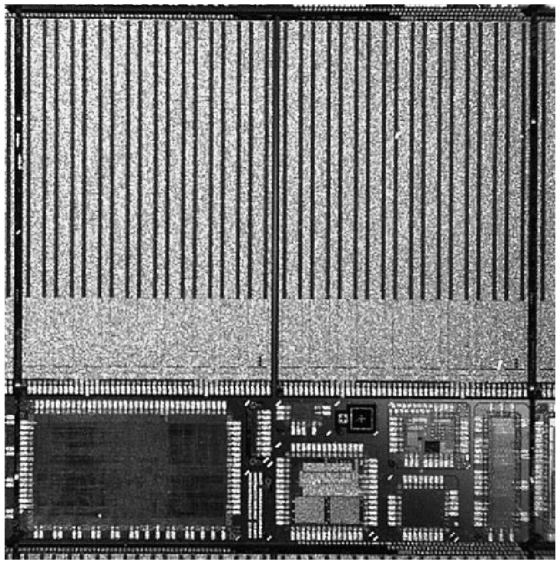
1.1.1.3 Pixel Electronics - Background

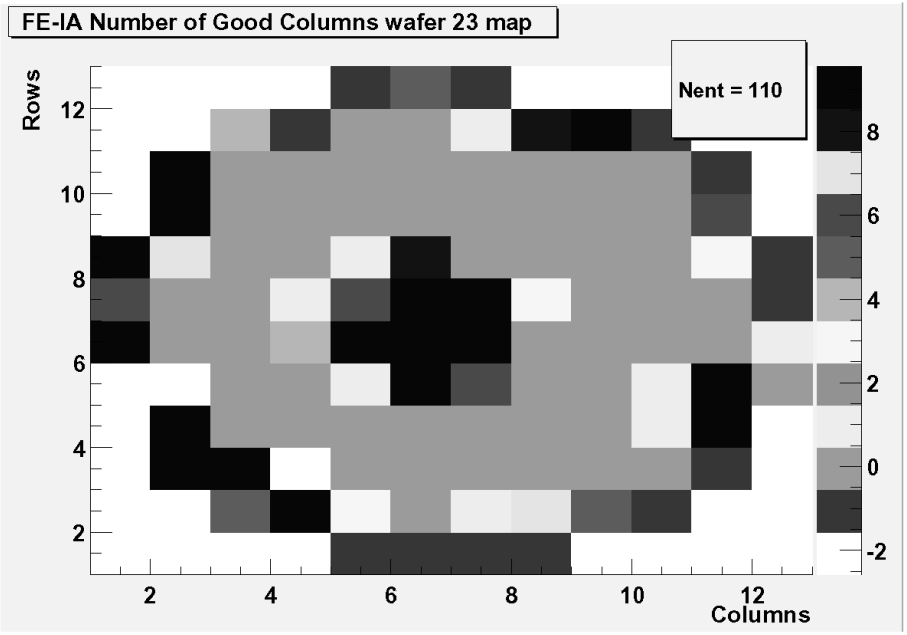
- History
  - Rad-soft ICs(HP) fabricated and tested extensively in lab and test beams. Proof-of-principle demonstrated already some years ago.
  - Conversion to rad-hard failed in DMILL(technical) and Honeywell(financial)
  - Transition to 0.25 micron technology(IBM or TSMC) made for all integrated circuits needed for project. IBM is baseline, TSMC is backup(also for test chips).
- ICs Required
  - FE – front-end chip, 16 per pixel module
  - MCC – Module control chip, one per module
  - VDC and DORIC – optical receivers and driver chips for conversion of optical ⇔ electrical signals
- K. Einsweiler remains overall ATLAS electronics coordinator and US has predominant role in electronics design.

1.1.1.3 – Pixel Electronics(I)

- Chips(reticle) on 12-wafer IBM run at right.
- Example wafer probe map for one type of FE chip is shown below.
- "Circle-of-death" pattern same on all wafers probed so far. Yield is about 15%. Similar pattern seen on CMS run(APV) done about same time => processing problem.







- Chips with no data appear White, bad Global Registers are Red, and other colors represent the Pixel Register test results. There are 18 (3) chips with working Global Registers and 9 (8) good column pairs in Pixel Register. This wafer was diced.

1.1.1.3 – Pixel Electronics(II)

- All blocks tested on FE chip and no major error in design, although a number of minor bugs.
- MCC chip design also looks good but has similar yield problem as FE.
- Optical chips(2nd generation) similarly good enough to proceed with opto-link testing this year. 3rd generation already submitted and 4th will be in April.
- Some wafers returned to IBM, negotiating for replacements.
- But yield is sufficient to carry out planned validation program this fiscal year.
- Extensive tests systems made(US responsibility) and will be used at multiple sites.
- We are proceeding to dice or bump/dice few wafers to make single chip-sensor assemblies, a few 16-chip modules and provide chips for optical testing.
- Extensive radiation and test beam program can now proceed.
- The successful fabrication of these chips, even with low yield, is a major step forward in the pixel project.

Pixel System

Near Term Schedule, Critical Path Items - ETC02

First IBM prototypes delivered	1/31/02	Done
Complete initial wafer probe	2/14/02	Done
First bump bonded assemblies	4/18/02	
Complete initial irradiation tests	8/15/02	
Second IBM prototype submitted	9/26/02	
Second IBM prototype wafers delivered	12/26/02	

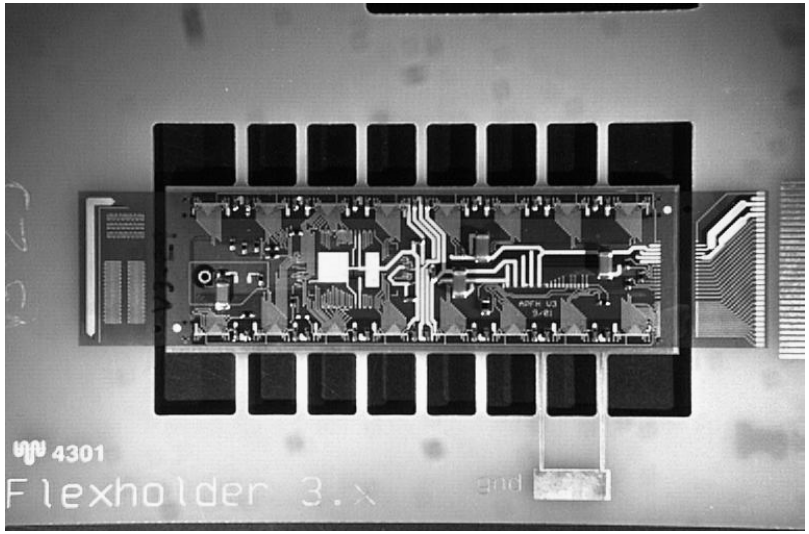
1.1.1.3 Pixel Sensors

- Production(about 25%) has been started with one vendor(CIS) and will be completed next month. CIS will then have a hiatus in production until about September, at which time production will resume.
- Additional pre-production started with 2nd vendor(Tesla). Full production planned to begin in September after additional post-rad qualification (no problems yet seen, but we have time to be careful).
- Production testing well established at multiple sites(New Mexico in US).
- Although start delayed, possible to maintain baseline schedule for completion of testing.
- Costs (including release of management contingency to begin production) at baseline estimates.

1.1.1.4 Hybrids

- Two generations of prototype optical hybrids(boards containing VCSELs and PIN diodes and optical ICs) have been made and tested(including irradiation) by OSU.
- Third generation fabricated and ready for testing this summer with IBM chips.
- Copper-on-kapton hybrids have been designed and fabricated (under direction of Oklahoma), tested(Albany and in Europe).
  - Third generation(3.x) fabricated successfully(compatible with rad-soft MCC)
  - Fourth generation(4.x) fabricated by one vendor and 2nd vendor about to start(compatible with IBM MCC)

Flex hybrid 3.x with components. Frame used for loading, transport (shipping covers not shown), testing and module assembly.



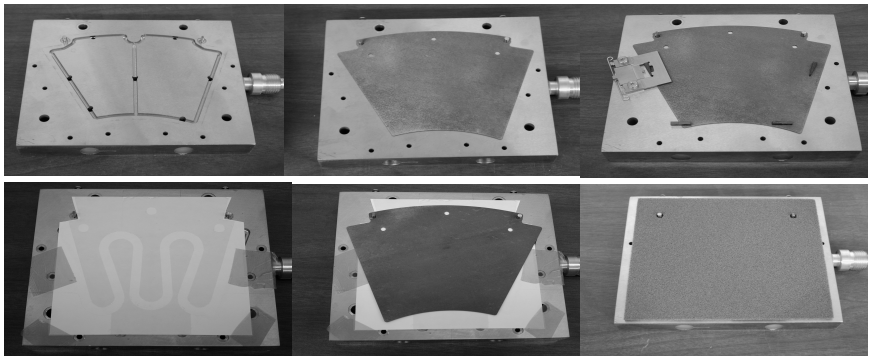
1.1.1.5 Pixel Modules

- Bump bonding with two vendors established.
- Transition to 8” wafers(IBM wafers) advanced with one vendor(IZM) and proceeding well with 2nd vendor(AMS).
- Thinning of 8” wafers to about 200 microns demonstrated but need more statistics to understand yield.
- Contracts in place to make about 100 modules(sum of mechanical dummies + active modules) this year. Roughly 5%(of active) scale test of module production chain.
- Procedures and tooling for module assembly advanced in Germany, Italy and US and will be debugged in course of building/testing 100 modules.
- M. Garcia-Sciveres(LBNL) has become overall ATLAS module coordinator.

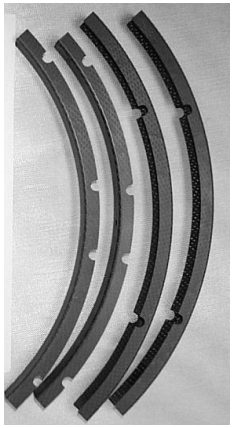
1.1.1.1 Mechanics(I)

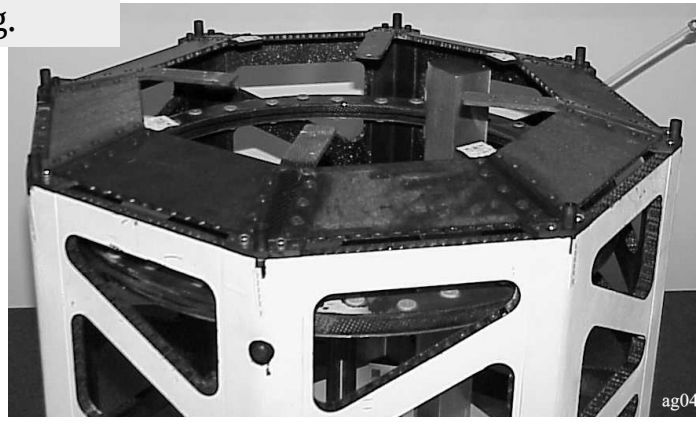
- Production started on disk sectors, to be completed this year.
- Contract let for pre-production disk support ring, going well, will be done next month and then production contract placed for completion by end this year.
- PRR passed for global support frame. Design complete. Procurement process started. Completion planned mid ’03.

Pre-production disk sectors being assembled.



Sections of pre-production disk support ring.





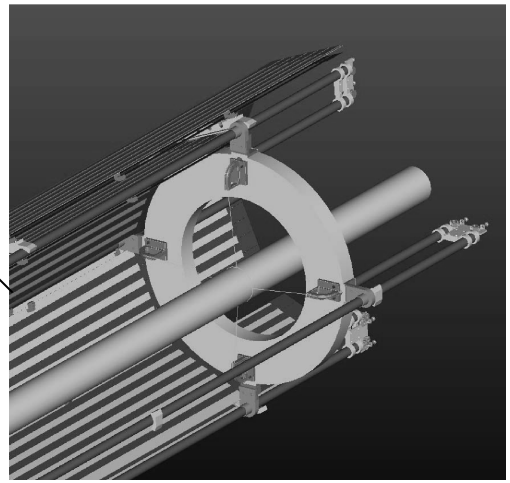
Global support and disk ring prototypes.

1.1.1.1 Mechanics(II)

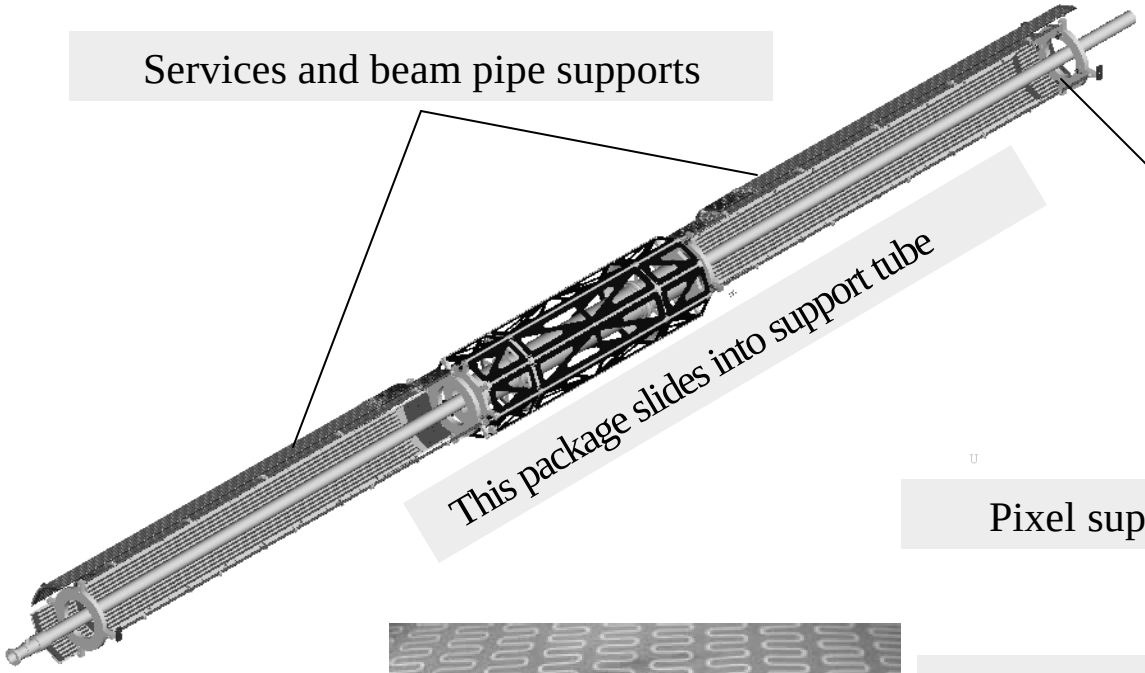
- See next page for figures
- Pixel support tube
  - Conceptual design review completed. FDR in June.
  - Prototype fabrication started to validate materials selection and demonstrate feasibility of bonding heaters to composite structures.
- Beampipe Support
  - Since US pixel baseline was established, design has evolved such that beampipe and pixel system are assembled on surface and lowered as package for insertion into support tube.
  - Beampipe now proposed to be supported from pixel services structure – this is addition to baseline design.
  - Funds granted to complete conceptual design to point that prototype can be built starting FY03.

Pixel Support Tube and Beampipe Support

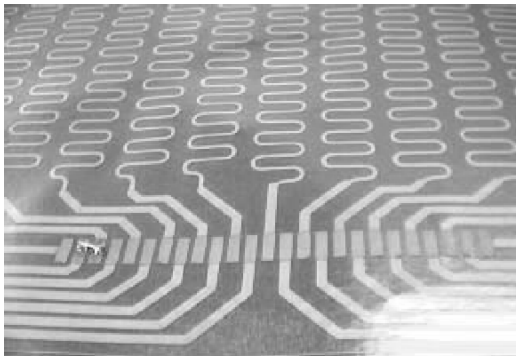
Services and beam pipe supports



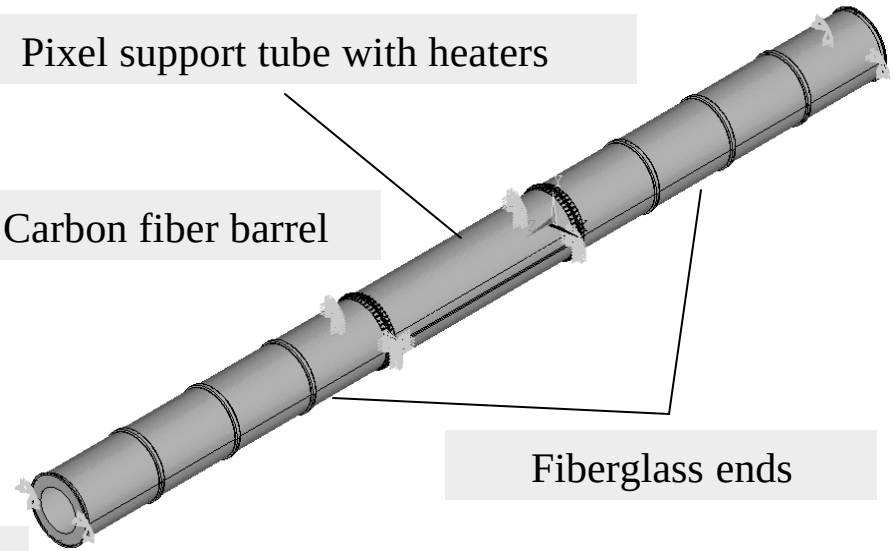
This package slides into support tube



Pixel support tube with heaters



Carbon fiber barrel



Fiberglass ends

Aluminum-on-kapton heaters

1.1.1 Pixels – Schedule

- Comparison of baseline vs. current schedule below.
- Electronics delay propagates into modules and final installation date.
- Completion of sensor production remains same, although start has been delayed. Ample capacity.
- Mechanics about on baseline schedule.

MILESTONE	BASELINE	CURRENT	DELTA
Start IBM Production	3/13/03	6/12/03	3 months
Start Trial Mech. Structure Assembly	4/9/03	4/8/03	0 months
Complete Sensor Production Testing	10/3/03	9/25/03	0 months
Start IBM Bare Module Production	10/22/03	1/29/04	3 months
Disk System at CERN	10/13/04	1/20/05	3 months
Ready for Installation	3/16/05	6/23/05	3 months
Need Date for Installation	4/15/05	10/15/05[1]	6 months

[1] Guess based on one-year delay in LHC. May be later.

1.1.2 Silicon Strips

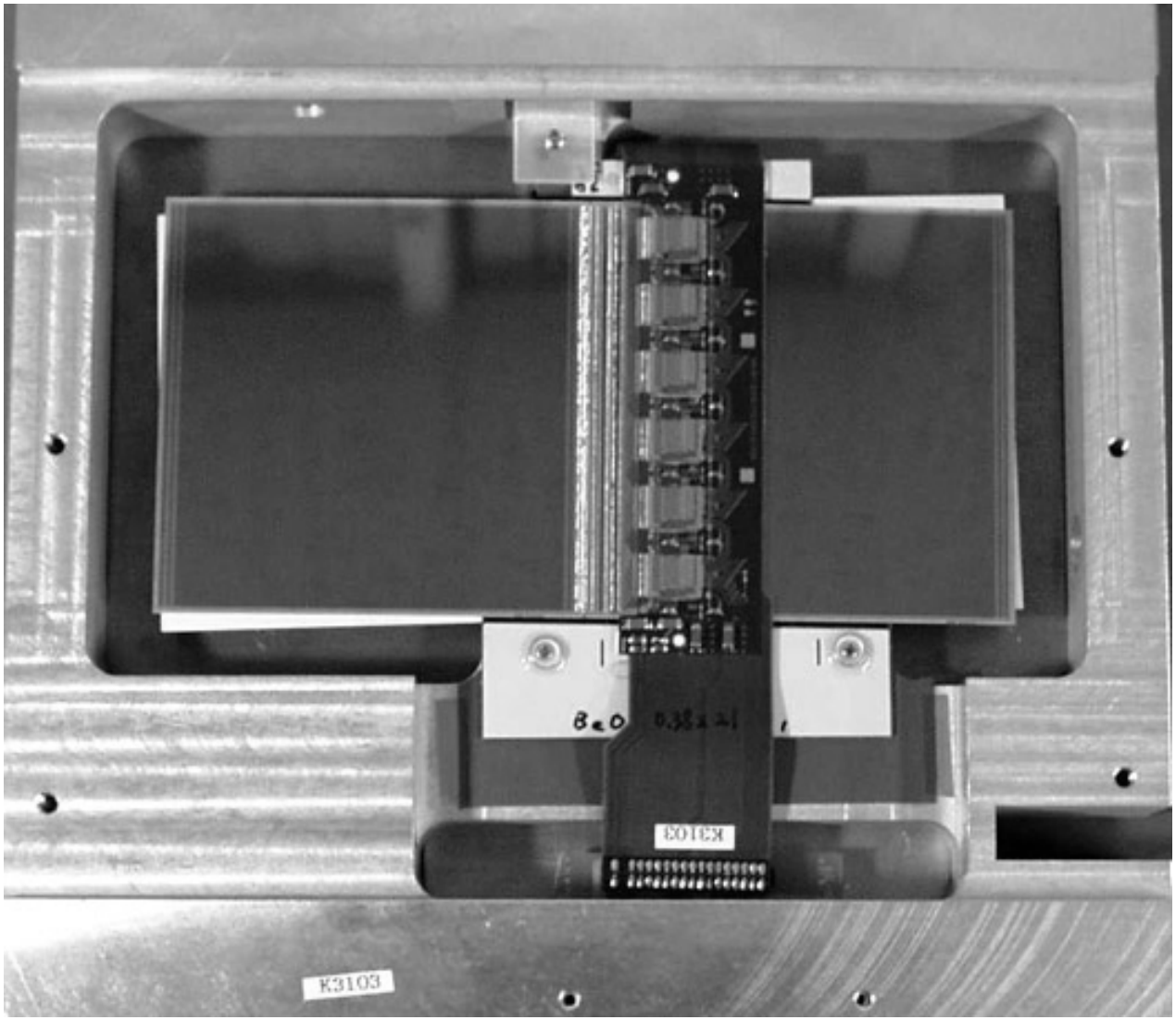
Baseline Deliverables:

- 45% of Frontend Chips.
- Testing of 50% of all Chips.
- Production and Testing of Hybrids for 670 Modules.
- Production and Testing of 670 Modules.

On or close to baseline schedule.

Also have Responsibility for:

- Electronics Coordination (from Frontends through Power Supplies).
- Systems Engineering (Mainly Grounding and Shielding Questions).


E3103

1.1.2.1 Frontend Chip Status

•Have requested and received Management Contingency allowing further chip purchase, bringing total U.S. contribution to 56% of total required to complete SCT construction. This accounts for cost increase in 1.1.2.

•Would like to bring this to our initial goal of 65% of total. Decision desired in May.

•Completion of all chip purchases, including spares is a very high priority since DMILL Process from ATMEL will likely not be available sometime next year. Company is anxious to complete the full fabrication.

•About 85% of the Chips for full construction have now been ordered.

Chip Testing

Chip Testing Milestones:		
10%	Complete	2/4/02
25%	Complete	3/28/02
50%	Complete	6/25/02
Production Testing	Complete	2/17/03

% Completed
13%
27%

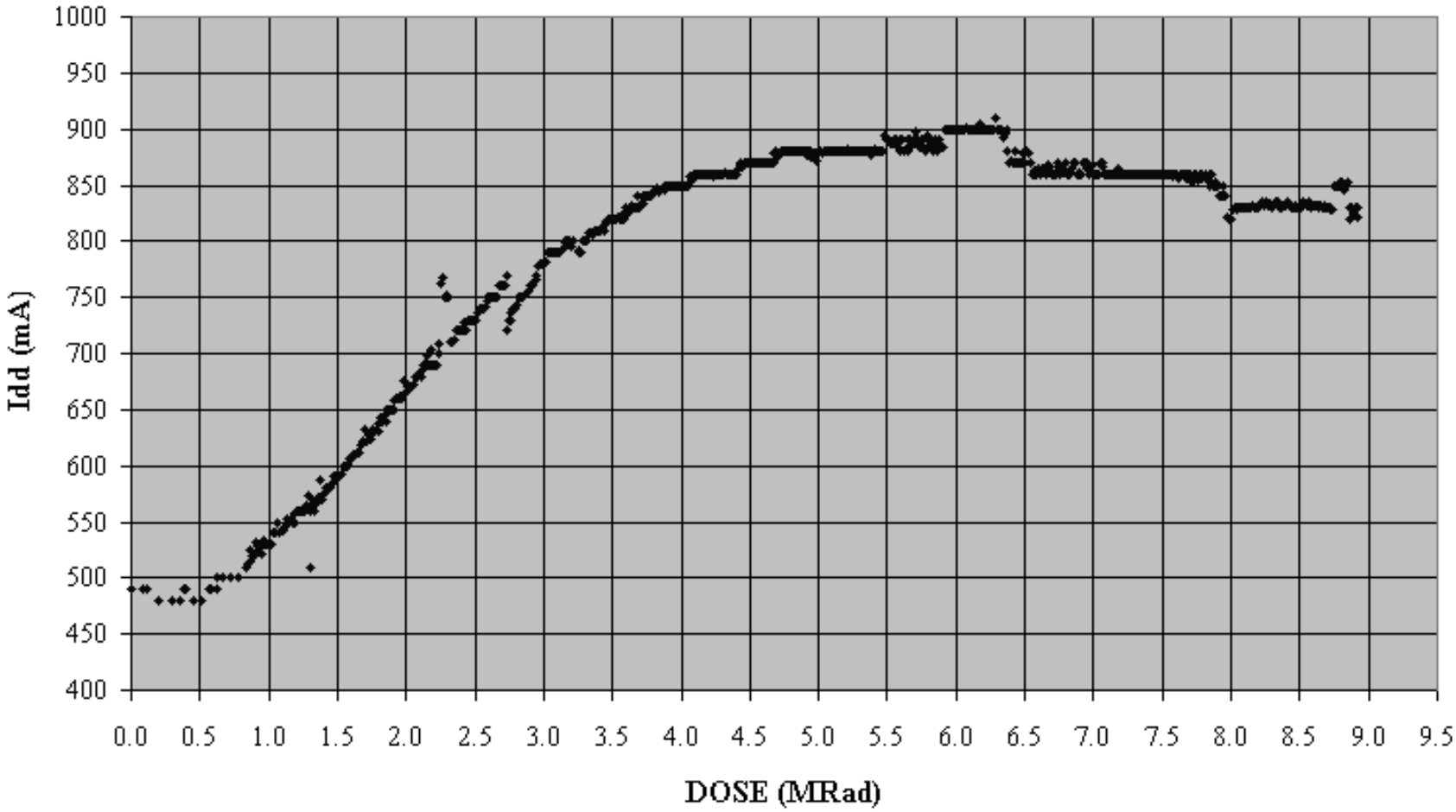
Goal for testing program: 5 Hours Per Wafer has been met.
Have two functioning probe stations at UCSC available for testing.

Idd Problem

One problem of a year ago was the somewhat out-of-spec leakage current seen for a number of chips in beam tests at CERN. The value of the Idd current has been shown to be dose rate dependent and should not be a problem for the real experiment. Data indicates that we will be below 1000mA limit. However, requires monitoring to be sure that behavior doesn't change for future fab. runs.

CERN has undertaken to do all x-ray tests of the delivered wafers to guarantee performance. We have taken over wafer testing of about 15% of the chips to allow them more time for x-ray testing.

We can do this without any additional cost.


12/13/01 - 3/8/02
Idd (mA)
1000
950
900
850
800
750
700
650
600
550
500
450
400
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
8.0
8.5
9.0
9.5
DOSE (MRad)

1.1.2.2 and 1.1.2.3 Hybrids and Modules

LBL tasks: assemble, bond and test, burn-in for modules.

UCSC tasks: repair, bond and test, burn-in for hybrids.

Schedule: Start Production 4/12/02

10%	complete	9/13/02	(3/week)
25%	complete	11/8/02	(2.5/day)
50%	complete	2/21/03	(2.2/day)
100%	complete	8/22/03	(2.5/day)

Status of Hardware

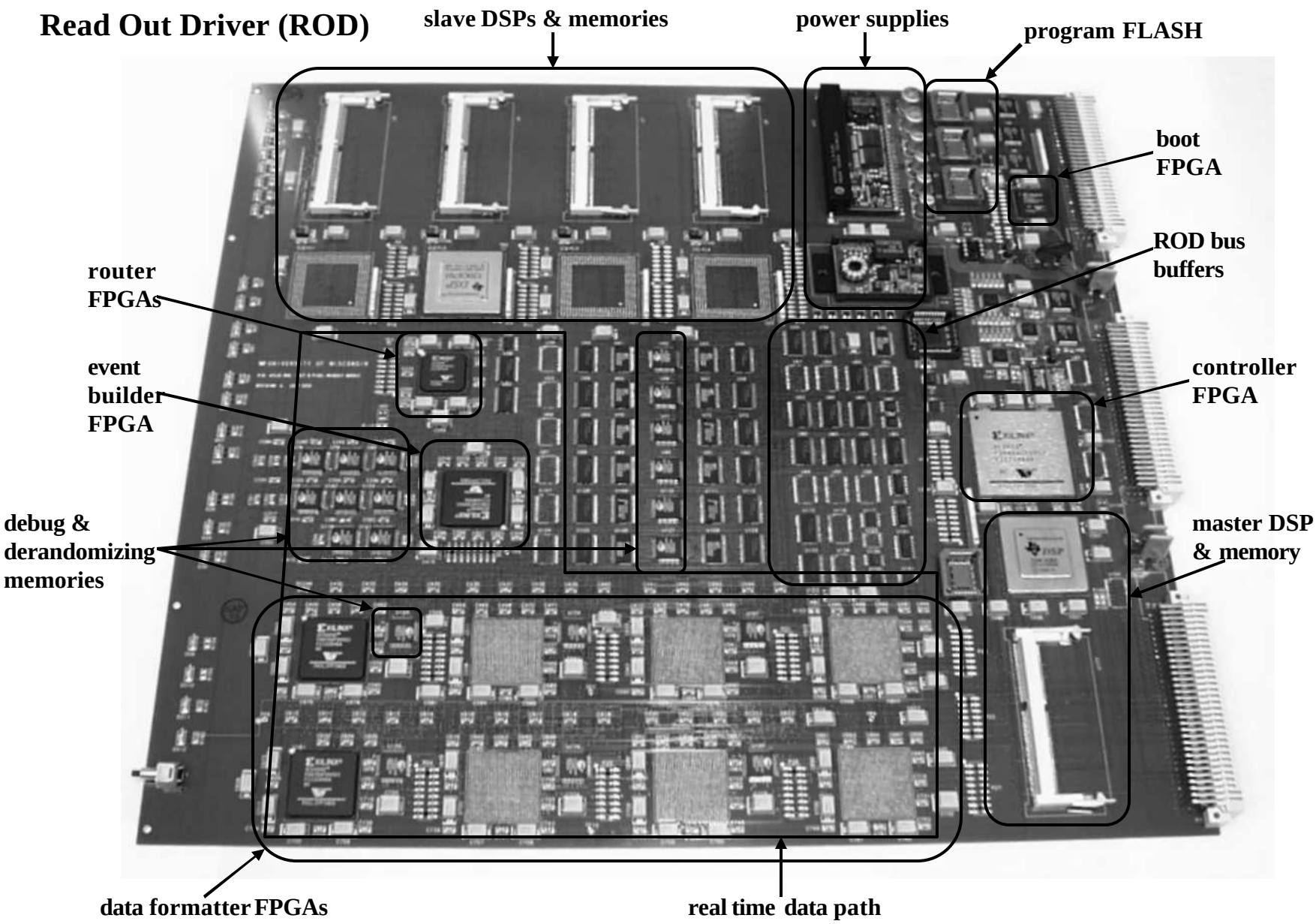
•Probe station in place and functioning for detector IV scans.

•Wafer Alignment System running. Numerous practice modules assembled and tested. Meets specifications.

•Initial fixtures complete. Need to order additional sets for several modules a day production rate.

•Qualification series of 5 modules begun. This is last step before start of production.

1.1.3 ROD (Read Out Driver)



ROD Status

Production model RODs (4 ea.) have been fabricated.
Yield on boards and loading is good.
Debugging is complete on four cards, minor upgrades below are being done.
These upgrades do not require new boards.
Cambridge has one production model ROD for system testing.
The other 3 RODs are presently at LBNL.
Parts and PC cards are in hand to assemble 9 more RODs

ROD Status

What hardware is working:

- Initialization working
- Controller FPGA is working
- Data Flow

  Through the Formatter, Event Fragment Builder and Router working
- Communication to/from Slave DSP working
- Running primitives in the Master/Slave DSP working
- VME read/write to the ROD working
- Can configure and trigger front end modules.

ROD Status

Upgrades needed:

VHDL upgrades needed to enable DMA to Master and Slave DSPs

VHDL to enable trapping of module configuration return data (pixels)

VHDL to provide ROD based counters of BCOs, Triggers and registers for event type related data for stand alone operation.

VHDL for recognition of fast command on the serial data streams from the master DSP via the controller to the front end modules.

VHDL for changes to the hardware memory map update

VHDL changes as needed for problems or future new requirements.

ROD Status

DSP Software Status

The DSP primitive software allows for Module/ROD/BOC configuration, triggering of modules and read out of events to the crate processor.

Interrupts working under BIOS and Texas Instruments (TI) library 1.2

DSP Software Upgrades Needed:

Upgrading to TI library 2.0

Improve the DSP processing of event data so it has event boundaries not number of word boundaries

Activate histogram packages in the slave DSP

Make changes the user community needs as testing advances.

Test Stand Software

The test stand software will be used for the early tests at Cambridge.

The test stand software is about 85% complete.

The remaining software is for the production test stand.

ROD Status

Projected schedule:

User evaluation from 2/02 till 5/02 is needed to have FDR of ROD.

The existing 4 RODs will be distributed to Oxford, Cambridge, and two in U.S.

Fabrication of remaining 9 RODs will follow FDR.

PRR should be 8/02 for fabrication of RODs (total of 100)

Concerns

SCT user evaluation in Europe urgently needed in next 2 months to maintain schedule for production of SCT RODs (baseline). Pixel evaluation will be done primarily in US and can likely meet schedule to request MC release this fall for pixel ROD production.

Installation

No specific technical responsibilities for SCT. Expect mostly to provide physicist participation.

For RODs, we have budgeted about 160k in total for FY02, FY03 and FY04 for technical help during installation at macro assembly sites.

Technical help for pixel installation required in FY05. Will involve mechanical, electrical and software support. 1 FTE for each task. Not yet in project budget. Estimated cost $655k.

Silicon Milestones Level 2

Level 2 Milestones

Subsystem	Schedule Designator	Description	ETC 01 Schedule Date	ETC 02 Schedule Date
Silicon	Sil L2/1	Start Full Silicon Strip Elec Prod	6-Jul-01	Complete
	Sil L2/2	Start Full Strip Module Production	7-Jan-02	12-Apr-02
	Sil L2/3	ROD Design Complete	1-Oct-01	17-Apr-02
	Sil L2/4	Compl Shipment of Silicon Strip Modules Prod	13-Oct-03	17-Oct-03
	Sil L2/5	ROD Production/Testing Complete	24-Jun-03	13-Mar-03
	Sil L2/6	Pixels 1st IBM Prototype Submitted	26-Jul-01	30-Nov-01
	Sil L2/7	Pixels Start IBM Production	13-Mar-03	12-Jun-03
	Sil L2/8	Pixels Start IBM Outer Bare Module Production	22-Oct-03	29-Jan-04
	Sil L2/9	Pixels 'Disk System at CERN'	13-Oct-04	20-Jan-05

Silicon Milestones Level 3

Level 3 Milestones (Goals)

Subsystem	Schedule Designator	Description	ETC 01 Schedule Date	ETC 02 Schedule Date
Silicon	Sil L3/1	Pixel System	13-Oct-04	20-Jan-05
	Sil L3/2	Silicon Strip System	13-Oct-03	17-Oct-03
	Sil L3/3	Read-Out Drivers	24-Jun-03	13-Mar-03

Silicon Milestones Level 4

Level 4 Milestones (Baseline Scope)						
WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC 01 Planned Completion Date	ETC 02 Planned Completion Date	ATLAS Required Date	ETC 02 Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Compl Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	-6
1.1.3	Sil L4/2	RODs 45% Production Compl	9/02	12/02	6/03	6
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	10/04	1/05	12/04	-1

WBS 3.1 Silicon System Commissioning, Maintenance and Operations, R & D

Abe Seiden
UC Santa Cruz

Overview

- Silicon system comprised of
  - -Pixel detector
  - -Silicon strip system (SCT)
  - -Read Out Drivers for these two systems
- U.S. deliverables are about 20% of total
- U.S. Institutions are also about 20% of total pixels+SCT
  - -Berkeley/LBNL
  - -Iowa State
  - -New Mexico
  - -Ohio State
  - -Oklahoma
  - -SUNY Albany
  - -UC Santa Cruz
  - -Wisconsin

Overview

Responsibilities for commissioning, maintenance and operations flow from:

- Construction Schedule.
- Responsibilities of U.S. Groups
- Development of Shared Facilities for long-term Maintenance.

Construction Schedule

Construction Project Time Schedule:

Pixels: Baseline 2-hit system ready for installation: 6/23/05

Strips: Completion of shipping of modules to England: 10/17/03

RODs: SCT RODs complete: 12/19/02

Pixel RODs complete: 3/13/03

Responsibilities: Pixel System

- Pixel System

  -Most of mechanics(support tube, support frame, disk region).

  -Large fraction of services(cables, piping, etc) within tracker volume.

  -About 20% of sensors(silicon detectors).

  -Major design role in IC electronics and system engineering, about 20% of procurement.

  -Most of hybrids.

  -Module assembly/testing about 25%.

Responsibilities: Silicon Strip(SCT) System

- Silicon Strip System

  -Major procurement of IC electronics, testing of these.

  -System management of entire electronics (front-ends to power supplies).

  -Systems engineering for electronics (grounding, shielding, cabling).

  -Construction of about one-third of barrel modules.

Responsibilities: Read Out Drivers

- Read Out Drivers

  -VME modules that read out both pixel and SCT modules.

  -Unique U.S. responsibility, all modules responsibility of U.S.

  -SCT RODs are to start fabrication in late FY02 for use at macro-assembly sites(where modules are put on mechanical structures).

  -Pixel RODs needed later, but possibly will be used for same purpose.

Near Term (FY 02, 03, 04)

Major M & O responsibilities for FY 02, 03, 04:

Spares and proportional contribution to shared facilities in SR building.

Spares in cases where obsolescence is an important factor, or where unique facilities are important:

FY02: $300k for spare SCT front-end chips. DMILL process from ATMEL is expected to soon not be available, therefore it is critical to buy spares. Would fund 8% spare chips.

FY03: $280k for 10% spare RODs.

FY04: $229k for 10% spare SCT modules (labor costs). Would follow completion of baseline deliverables, while facilities and personnel are available.

Near Term (FY 02, 03, 04)

SR building, shared facilities, for long term servicing of the tracker. Some required items: clean room; piping, cooling and ventilation; electrical items such as fiber optics, connectors PC's, racks. Cost estimates based on work of Inner Detector Steering Group.

U.S. Share of Costs:

FY03	FY04
$108k	$267k

Estimated additional costs in FY 04 and 05 are $427k to complete facilities.

Near Term

A shortage in M&O funds will leave us unable to complete the spares, which will be important for the long term operation of the detector, and unable to contribute our proportional share to the SR building, which is being jointly funded by all the institutions involved in the detector construction.

Longer Term

For SCT and RODs expect to be mainly involved in M&O starting in FY05. For Pixels starting in FY06.

M&O responsibilities will follow construction responsibilities. Also expect some “spikes” in activity when major repairs occur. For example, can expect such increases in activity during an early shut-down soon after start-up and then during a more major intervention after several years of running.

M&O Plan: Pixels(WBS 3.1.1)

-Spares are not currently included in this estimate. We assume there will be relatively rapid upgrade of the pixel system.
-We have projected continued support of unique U.S. deliverables in mechanics that allow removal/re-insertion of the pixel system (ME and some tech support).
-We have provided for minimal continued support of electronics (EE and some tech support).
-We have also included technical support for the general operations/ maintenance pool(note that there is currently no CERN involvement in the pixel system => technical support from outside Cern likely to be greater than other systems).
-And we have included software support for DAQ, calibration monitoring, etc.

M&O Plan: Strips(WBS 3.1.2)

-Systems engineering(N. Spencer from UCSC) has been vital. Continued systems engineering will be needed during pre-operations(after modules are installed on support structure at Oxford), during surface testing at CERN and during commissioning.

-Continuation of some systems engineering support is expected during initial operations, primarily in FY06 and FY07, and then at a small level.

-Proportional US contribution to technical support pool will be required.

-There are likely to be minor equipment expenses that we believe will be shared across all institutions/countries.

M&O Plan: RODs(3.1.3)

-The RODs are a unique US responsibility so all operations and maintenance is assumed to be provided by the US.
-The manpower levels to achieve this are shown on the next page.

M&O Personnel Summary

	FY05	FY06	FY07	FY08	FY09
Pixels (WBS 3.1.1)					
Mech. Eng.		1.0	1.0	1.0	0.4
Elect. Eng.		1.0	0.5	0.5	0.2
Technician		1.5	1.8	1.8	1.4
Software		1.0	1.0	1.0	1.0
Designer		0.5			
SCT (WBS 3.1.2)					
Elect. Eng.	0.6	1.1	0.5	0.1	0.1
Technician	1.3	1.3	2.3	1.0	1.0
RODs (WBS 3.1.3)					
Elect. Eng.	1.0	1.0	1.0	0.5	0.1
Technician			0.3	0.3	0.3
Software	0.3	0.3	0.3	0.1	0.1

Longer Term

Budget estimate for longer term M&O:

FY05	FY06	FY07	FY08	FY09
0.875M	1,674M	1,498M	1,161M	0.856M

Costs assumed largest at turn-on as we learn how to use the detector and make initial repairs

R & D for Silicon Tracking

Expect to focus:

- Primarily on Pixel R & D, since this system is likely to be significantly expanded in area covered in any tracking upgrades.
- Front-end electronics options for silicon, since this evolves rapidly over time.

Pixel R&D

- The useful lifetime of the innermost pixel layer is expected to be limited to a few years at design luminosity. However, there are substantial uncertainties in the actual radiation levels and realistic operating voltages => plan on replacing early, since this layer is required for all b-tagging.
- On a somewhat longer timescale, luminosities beyond 10^{34} will require major upgrades to the tracking system, eg. replacement of gas detectors by silicon, replacement of silicon strip detectors by pixels, and increased radiation hardness(beyond the current 25MRad) for pixel detectors.
- R&D for $>10^{34}$ is very challenging(it's taken us about 20 years to be comfortable with 10^{34}).

Pixel R&D Areas

- **Electronics**
  - Increase/understand radiation hardness > 100 MRad. This looks promising but much more study needed.
  - Follow the technology from 0.25μ to smaller feature sizes. Work on 0.13μ will begin soon at CERN.
  - Reduce pixel size below 50x400μ. There is already significant confusion in at least innermost pixel layer.
- Sensors
  - A follow on to the successful ROSE collaboration is starting to address the 10^{35} challenge.
- Hybridization
  - Reduce the pitch of bump bonding to allow smaller pixels.
  - Development of MCM-D technology to mostly eliminate kapton hybrids has been ongoing for some time and needs further development.
- **Mechanics and systems issues**
  - Reduce material and complexity of the mechanics/cooling. Material reduction directly improves electron and photon energy resolution and tracking performance.
  - Complexity of current cabling/cooling is formidable. Reliability will be problem.
  - Radioactivation of pixel elements is already significant at 10^{34}. There are as yet no good ideas about how to handle this for higher luminosities.
- US ATLAS does not have the resources to address all of these issues, so our planning has focused on the **underlined areas**.